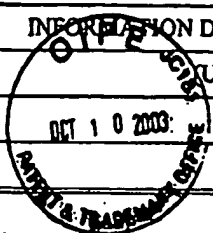


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RF	AB	5,630,051	5/13/97	Sun et al.	395	183.08			
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RF	AD	5,623,499	4/22/97	Ko et al.	371	22.1			
RF	AE	5,654,657	8/5/97	Pearce	327	163			
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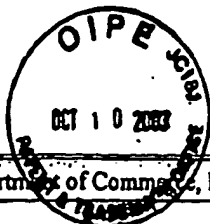
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PART "B"

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Sheet 8 of 24

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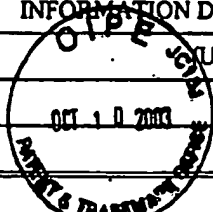
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PART "B"

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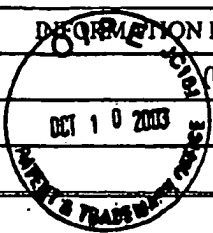
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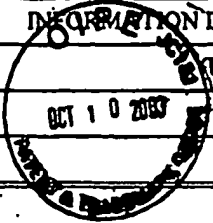
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RF	AI	Aharon, A., et al., "Test Program Generation for Functional Verification of PowerPC Processors in IBM", 32 nd Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 279-285.							
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RF	AN	Bryant, R. E., "Binary Decision Diagrams and Beyond: Enabling Technologies for Formal Verification", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, November 5-9, 1995, pp. 236-243.							
RF	AO	Hoskote, Y. V., et al., "Automatic Verification of Implementations of Large Circuits Against HDL Specifications", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 3, March 1997, pp. 217-228.							
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PART "B"

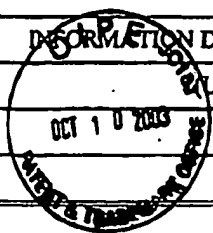
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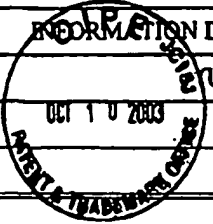
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RF	AI	Goel, P., "An Implicit Enumeration Algorithm to Generate Tests for Combinational Logic Circuits", IEEE Transactions on Computers, Vol. C-30, No. 3, March 1981, pp. 215-222.					
RF	AJ	Jones, R., et al., "Self-Consistency Checking", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 158-171.					
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RF	AL	McMillan, K. L., "Fitting Formal Methods into the Design Cycle", 31 st Design Automation Conference, San Diego, CA, June 6-10, 1994, pp. 314-319.					
RF	AM	Geist, D., et al., "Coverage-Directed Test Generation Using Symbolic Techniques", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 142-159.					
RF	AN	Motohara, A., et al., "A State Traversal Algorithm Using a State Covariance Matrix", 30 th Design Automation Conference, Dallas, Texas, June 14-18, 1993, pp. 97-101.					
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RF	AJ	Sangiovanni-Vincentelli, A., "Verification of Electronic Systems", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 106-111.						
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RF	AL	Chung, Pi-Yu, "Diagnosis and Correction of Logic Design Errors in Digital Circuits", 30 th Design Automation Conference, Dallas, Texas, June 14-18, 1993 pp. 503-508.						
RF	AM	Chandra, A. K., "Architectural Verification of Processors Using Symbolic Instruction Graphs", IEEE International Conference on Computer Design, 1994, pp. 454-459.						
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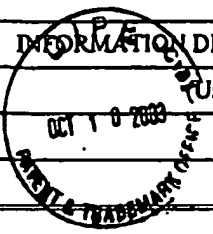
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RF	AJ	Monaco, J., "Functional Verification Methodology for the PowerPC 604™ Microprocessor", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 319-324.					
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RF	AK	Offutt, A. J., et al., "An Experimental Evaluation of Data Flow and Mutation Testing", Software-Practice and Experience, Vol. 26(2), February 1996, pp. 165-176.							
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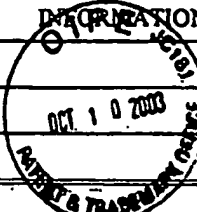
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RF	AJ	Knapp, D., et al., "Behavioral Synthesis Methodology for HDL-Based Specification and Validation, 32 nd Design Automation Conference, San Francisco, CA June 12-16, 1995, pp. 286-291.						
RF	AK	Tomita, M., et al., "Rectification of Multiple Logic Design Errors in Multiple Output Circuits", 32 nd Design Automation Conference, San Diego, CA, 1994 pp. 212-217.						
RF	AL	Kam, Timothy, et al., "Implicit State Minimization of Non-Deterministic FSM's", International Conference on Computer Design: VLSI in Computers & Processors, Austin, TX, October 2-4, 1995, pp. 250-257.						
RF	AM	Bryant, R. E., et al., "Verification of Arithmetic Circuits with Binary Moment Diagrams", 32 nd Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 535-541.						
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RF	AI	Swamy, G., et al., "Incremental Methods for FSM Traversal", International Conference on Computer Design: VLSI in Computers & Processors, Austin, TX, October 2-4, 1995, pp. 590-595.					
RF	AJ	Cyrluk, D. A., et al., "Theorem Proving: Not an Esoteric Diversion, but the Unifying Framework for Industrial Verification", International Conference on Computer Design: VLSI in Computers & Processors, Austin, TX, October 2-4, 1995, pp. 538-544.					
RF	AK	Swamy, G. M., et al., "Incremental Formal Design Verification", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, November 6-10, 1994, pp. 458-465.					
RF	AL	Butler, K. M., "Heuristics to Computer Variable Orderings for Efficient Manipulation of Ordered Binary Decision Diagrams", 28 th ACM/IEEE Design Automation Conference, San Francisco, CA, June 17-21, 1991, pp. 417-420.					
RF	AM	Rudnick, E. M., et al., "Sequential Circuit Test Generation in a Genetic Algorithm Framework", 31 st Design Automation Conference, San Diego, CA, June 6-10, 1994, pp. 698-704.					
RF	AN	Wing, J. M., "A Specifier's Introduction to Formal Methods", Computer, Vol. 23, No. 9, September 1990, pp. 8-24.					
RF	AO	Keen, J. "Specification for Duplo SNaC RLT Assertion Language", December 6, 1996.					
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RF	AJ	Golson, S., "State Machine Design Techniques for Verilog and VHDL", http://www.synopsys.com/pubs/JHLD/JHLD-099401 , believed to be prior to October 1997.						
RF	AJ	Schroeder, S., "Turning to Formal", Integrated System Design, September 1987, pp. 15-20.						
RF	AK	Panda, S., et al., "Symmetry Detection and Dynamic Variable Ordering of Decision Diagrams", IEEE/ACM International Conference on Computer-Aided Design, November 6-10, 1994, pp. 628-631.						
RF	AL	Iwashita, H., et al., "CTL Model Checking Based on Forward State Traversal", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, November 6-10, 1996, pp. 82-87.						
RF	AM	Hojati, R., et al., "Verification Using Uninterpreted Functions and Finite Instantiations" Formal Methods in Computer-Aided Design, First International Conference FMCAD '96, Palo Alto, CA November 6-8, 1996, pp. 218-233.						
RF	AN	Narayan, A., et al., "Partitioned ROBDDs - A Compact, Canonical and Efficiently Manipulable Representation for Boolean Functions", IEEE/ACM International Conference on Computer-Aided Design, November 6-10, 1996, pp. 547-554.						
RF	AO	Zhou, Z., "Formal Verification of the Island tunnel Controller Using Multiway Decision Graphs", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 218-232.						
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RF	AK	Cho, H., et al., "A Structural Approach to State Space Decomposition for Approximate Reachability Analysis", IEEE International Conference on Computer Design: VLSI in Computers and Processors, Cambridge, MA, October 10-12, 1994, pp. 236-239.					
RF	AL	Cho, H., et al., "A State Space Decomposition Algorithm for Approximate FSM Traversal", IEEE, 1994, pp. 137-141.					
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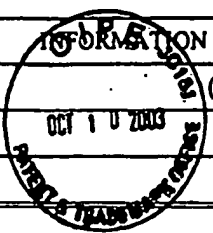
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RF	AJ	Ganapathy, G., et al., "Hardware Emulation for Functional Verification of K5", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 315-318.							
RF	AK	Sawant, S., et al., "RTL Emulation: The Next Leap in System Verification", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 233-235.							
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RF	AM	Narayan, S., et al., "Interfacing Incompatible Protocols using Interface Process Generation", 32 nd Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 468-473.							
RF	AN	Monohan, Chuck, et al., "Symbolic Modeling and Evaluation of Data Paths", 32 nd Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 389-394.							
RF	AO	Marculescu, D., et al., "Stochastic Sequential Machine Synthesis Targeting Constrained Sequence Generation", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 696-701.							
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	AG						Yes No
	AH						Yes No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Verlind, E., et al., "Efficient Partial Enumeration for Timing Analysis of Asynchronous Systems", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 55-58.					
RF	AJ	Popescu, V. et al., "Innovative Verification Strategy Reduces Design Cycle Time For High-End SPARC Processor", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 311-314.					
RF	AK	Casaubieilh, F., et al., "Functional Verification Methodology of Chameleon Processor", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 421-426.					
RF	AL	Brown, S., et al., "Experience in Designing a Large-scale Multiprocessor using Field Programmable Devices and Advanced CAD Tools", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 427-432.					
RF	AM	Norris, C., "State Reduction Using Reversible Rules", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 564-567.					
RF	AN	Sanghavi, J., et al., "High Performance BDD Package By Exploiting Memory Hierarchy", 33 rd Design Automation Conference, Las Vegas, NV, 1996, pp. 635-640.					
RF	AO	Meyer, W., et al., "Design and Synthesis of Array Structured Telecommunication Processing Applications", 34 th Design Automation Conference, Anaheim, CA, June 9-13, 1997, pp. 486-491.					
Examiner		RUSSELL FREED		Date Considered		1. 12. 05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

PART "B"

Sheet 23 of 24

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket N .		Serial No.	
				01N0061CUS		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.			
(Use several sheets if necessary)							
				Filing Date		Group 2128	
				MAY 4, 2001		-2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Seawright, A., et al., "A System for Compiling and Debugging Structured Data Processing Controllers", EURO, Design Automation Conference, 1996.					
RF	AJ	Data Sheet "ATC's CoverMeter™ USA Commercial Price List, 1996.					
RF	AK	Dill, D. L., et al., "Acceptance of Formal Methods: Lessons From Hardware Design", Computer, April 1996, pp. 23-24.					
RF	AL	Bullis, D., "Verification and Modeling for Synthesis-Based Design", Marketing Communications, believed to be prior to 1997, pp. 15-17.					
RF	AM	Article "Product expectations in networking have risen to a point where systems must be self-correcting. The added cost of 'safe' design practices is not even questioned", Electronic Engineering Times, November 11, 1996, p. 48.					
RF	AN	Young, L. H., "Building A Better Bug Trap", Electronic Business Today, November 1996, pp. 49-53.					
RF	AO	Silbey, A. "The Systems Challenge for EDA Tools" Viewlogic Systems, believed to be prior to October 1997, pp. 22-26.					
Examiner		Russell FRETZ		Date Considered		1.12.05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				01N0061C US		09/849,005	
				Applicants: Chian-Min Ho et al.			
				Filing Date		Group 2128	
				MAY 4, 2001		-2123-	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
21	AI	Singer, S., et al., "Next Generation Test Generator (NGTG) for Digital Circuits", AUTOTESTCON, 97, 1997 IEEE Autotestcon Proceedings, Septe. 22-25, 1997, pp. 105-112.					
	AJ						
	AK						
	AL						
	AM						
	AN						
	AO						
Examiner		Russell FRETZ		Date Considered		1.12.05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							